University of Engineering and Technology Taxila

Sub Campus Chakwal

End Semester Examination (Spring 2013) 2K11 Electronic Engineering (4th Semester)

Course Title: Microprocessors and Microcontrollers

	ROII #						
Note:-Erased and overwritten answers will be considered as wrong.							
Q.	1 (a).Only encircle	the appropriate a	nswer. (15 Marks)				
1)	Which of the following a) ISA	b) EISA	c) PCI Express	d)VESA			
2)	The resident local bus is often called the						
ĺ			c) PCI bus	d) control bus			
3)	8086 is a 16-bit microprocessor with a bit data bus.						
	a) 6	b) 16	c) 32	d) 8			
4)	8284A is what?						
	a) DMA Controller	b) Buffer	c) Clock Generator	d) Timer			
5)	Each Bus Cycle consists of clock periods.						
ŕ	a) 4	b) 3	c) 2	d) 1			
6)	When a memory chip a) Give a 0 b) Give a 1 c) Are at high imped d) Do not change		is not selected) then its data	a lines?			
7)	A 2764 EPROM will have memory						
	a) 8K X 8	b) 4K X 8	c) 32K X 8	d) 16K X 8			
8)	After hardware reset, the 8088 picks up code form location (cold start).						
	a) FFFFF	b) FFFF0	c) 0000F	d) 11111			
9)	The two instructions to a) Bound/un-Bound		etween an I/O device and pr				

Total Marks: 40

Time Allowed: 45 mins

10)	A method of I/O control called		_ synchronizes the I/O device with the			
		croprocessor.				
	a)	handshaking	b) buffering	c) latching	d) Both b & c	
11)	Th	e divide error inte	errupt is			
	a)	Type 0	b) Type 2	c) Type 3	d) Type 4	
12)) Th	e pin of Al	DC080X is pulsed to i	indicate the start of conv	version.	
	a)	RD	b) INTR	c) WR	d) CS	
13)) Wl	nich of the following	ng is a one-byte interr	rupt instruction?		
	a)	BOUND	b) INT3	c) INT4	d) RET	
14)) Ho	ow many interrupt	vectors are there?			
	a)	16	b) 64	c) 256	d)512	
15)			o address pins connec ddress this I/O device	tions A_0 and A_1 , how m?	any I/O addresses	
	a)	16	b) 1	c) 2	d) 4	
\mathbf{Q}_1	1 (b). Identify True	e ☑ and False ☑ S	Statements. (5 Mar	ks)	
1) An interrupt vector contains the address (segment and offset) of the interprocedure.					f the interrupt service	
	2)	The DMA I/O tec		t access to the memory	while the	
	3)	•	temporarily disabled.	address bits above A_{15} a	ore undefined for I/O	
	3)	instructions.	5-bit 1/O address. The	address ons above A ₁₅ a	re undermed for 1/O	
	4) A parity error indicates the start and stop bits are not in their proper places.					
	5)	A DMA write tra	insfers data from an I/	O device to memory.		
	1 (c ark		nswers to followir	ng questions in less	than 4 lines (20	
1)	Wl	hat is a Wait State	$(T_{\rm w})$?			
ĺ			· · · · /			
2)		ow do we separate a	address from data in p	rocessor where both are	shared on the same	

3)	In I/O instructions what does the term fixed and variable address mean?
4)	Differentiate between isolated and memory mapped I/O?
5)	What is overrun error in serial communication?
6)	An 8-bit ADC has 5 volts of V_{ref} . Find its resolution (The minimum change in input-voltage to cause an increment in digital value). Also what will be digital output when input is 5V.

7)	What are three modes of serial communication?	
8)	What is the role of first/last flip flop in 8237 DMA controller?	
9)	What is noise immunity? What is Fanout?	
10)	What is minimum and maximum mode of microprocessor?	